

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25	(US-5404395-\$ or US-5970059-\$ or US-5978386-\$ or US-5621896-\$ or US-5014264-\$ or US-5297141-\$ or US-5327492-\$ or US-5386689-\$ or US-5532898-\$ or US-5581660-\$ or US-5594777-\$ or US-5644754-\$ or US-5696660-\$ or US-5777836-\$ or US-5783999-\$ or US-5950195-\$ or US-5991631-\$ or US-6025738-\$ or US-6031835-\$ or US-6055236-\$ or US-6061220-\$ or US-6111883-\$ or US-6115701-\$ or US-6192409-\$ or US-3665510-\$).did.	USPAT	AND	ON	2007/12/20 17:58
L4	2	L1 (status or switch\$4)(interrupt)(back\$4 or trigger\$) same(control\$4 or supervis\$4 or monitor\$4 or switch\$4)	USPAT	AND	ON	2007/12/20 18:01
L5	2	L1 (status or switch\$4)(interrupt)(back\$4 or trigger\$) same(control\$4 or supervis\$4 or monitor\$4 or switch\$4)	US-PGPUB; USPAT; IBM_TDB	AND	ON	2007/12/20 18:01
L6	2	L1 (status or switch\$4)(interrupt)(back\$4 or trigger\$) same(control\$4 or supervis\$4 or monitor\$4 or switch\$4)	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:17
L7	1	"20040103304"	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:03
L8	15	tong near shao.in.	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:04
L9	1415	(713/100).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/12/20 18:05
L10	219	(380/257,287).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/12/20 18:05
L11	1457	(726/26).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/12/20 18:05

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L12	1482	(710/260,264).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/12/20 18:16
L13	4552	L9 or L10 or L11 or L12	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2007/12/20 18:06
L14	44	L13((status or switch\$4)(interrupt)(back\$4 or trigger\$\$) same(control\$4 or supervis\$4 or monitor\$4 or switch\$4)).clm.	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:06
L15	16	L1 ((switch\$4 or status)same(internal or inside or outside or first))	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:08
L16	15	L15(internal or inside or outside or first)same(second or outside or external)same(switch\$4 or status or interrupt)	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:11
L17	24	L14(internal or inside or outside or first)same(second or outside or external)same(switch\$4 or status or interrupt).clm.	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:16
L18	5	L17 (NMI)	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:09
L19	0	L16 (NMI)	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:10
L20	2887	L9 or L12	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2007/12/20 18:16
L21	171	L20(internal or inside or outside or first)same(second or outside or external)same(switch\$4 or status or between)same(quick\$\$ or interrupt).clm.	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:17
L22	17	L21((back\$4 or trigger\$\$) same(control\$4 or supervis\$4 or monitor\$4 or switch\$4)).clm.	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:23

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L23	1	L22 (NMI)(back\$4 adj (up))same(supervis\$4 or switch\$4 or control\$4 or monitor\$4)	US-PGPUB; USPAT; EPO; IBM_TDB	AND	ON	2007/12/20 18:24
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NMI status switching OR back * up controlling 1996 - 2003

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[K Johnson](#)

[A Nouri](#)

[R Molloy](#)

[D White](#)

[S Clough](#)

Computer system with function for **controlling** system configuration and power supply **status** data - all 3 versions »

K Uehara, T Inomata - US Patent 5,754,798, 1998 - Google Patents

... Since an instruction of **switching** of the system operation ... ISSUE READ PS **STATUS** (80)/

READ BATTERY CAPACITY ... ISSUE **BACK**-LIGHT CONTROL IB *) COMMAND IN ACCORDANCE ...

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Communication apparatus for **controlling switching** between a normal mode and a power saving mode - all 3 versions »

T Miyazaki, M Momose, S Kohri, N Nakamura, Y ... - US Patent 5,933,581, 1999 - Google Patents

... [54] COMMUNICATION APPARATUS FOR **CONTROLLING SWITCHING** BETWEEN A NORMAL MODE AND A POWER SAVING MODE ... S41 SEND REQUESTED **STATUS BACK** ... SEND **STATUS** REQUEST COMMAND ...

[Cited by 5](#) - [Related Articles](#) - [Web Search](#)

Communication apparatus having a printer **controlling** recording in accordance with a bilateral record ... - all 3 versions »

T Miyazaki, M Momose, S Kohri, N Nakamura, Y ... - US Patent 5,819,013, 1998 - Google Patents

... START INSTRUCT WAKE-UP OF PRINTER IN ESS MODE WAIT FOR 200msec ... 6, 1998 Sheet 16 of

21 5,819,013 SEND 80H **BACK** SET HIGH ORDER TIME DATA SEND **STATUS 0 BACK** ...

[Cited by 6](#) - [Related Articles](#) - [Web Search](#)

The **NMI** Absorbed-Dose-to-Water Calorimeter (A **Status** Report) - all 2 versions »

M Pieksma, E Van Dijk, AHL Aalbers - Proceedings of the International Workshop on Recent Advances ..., 2000 - npl.co.uk

... The history of calorimetry at the **NMI** goes **back** to 1977 ... absorbed dose to water standards

of the **NMI** and the ... Williams AJ and Rosser KE 1998 A **status** report on ...

[Cited by 3](#) - [Related Articles](#) - [Web Search](#)

Monitoring an Automated System for a Single Failure: Vigilance and Task Complexity Effects. - all 3 versions »

R Molloy, R Parasuraman - Human Factors, 1996 - questia.com

... the participant responded immediately moved **back** to the ... a decrement when the engine **status monitoring** task was ... 747-SP, N4522V, 300 nautical miles northwest of ...

[Cited by 45](#) - [Related Articles](#) - [Web Search](#)

Computer-**controlling** life support system and method for mixed-gas diving - all 3 versions »


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[M Rostoker](#)
[D Boyle](#)
[R Hausman](#)
[P Sherer](#)
[J Rivers](#)

Single chip multiprocessor architecture with **internal task switching** synchronization bus - all 5 versions »

MD Rostoker, DB Boyle - US Patent 5,761,516, 1998 - Google Patents

... [45] Date of Patent: [54] SINGLE CHIP MULTIPROCESSOR ARCHITECTURE WITH

INTERNAL

TASK SWITCHING SYNCHRONIZATION BUS ... B: O INTERRUPT 1 INTERRUPT 2

STATUS (32 BIT) ...

Cited by 48 - [Related Articles](#) - [Web Search](#)

Communications interface adapter for a computer system including posting of system **interrupt status** - all 3 versions »

SF Gates, J Davoudi - US Patent 6,085,278, 2000 - Google Patents

... to normal command completions or an event- related **interrupt** such as expiration of an **internal** timer or ... The **interrupt posting status** registers 322 ...

Cited by 14 - [Related Articles](#) - [Web Search](#)

Communication resource allocation by **interrupt status** - all 2 versions »

DJ McDonald, JA Wolfe, HR Wolf - US Patent 5,638,055, 1997 - Google Patents

... ALLOCATION BY **INTERRUPT STATUS** ... needs to **interrupt** a call to deliver an important ...

by examining an **internal** database that tracks the current ...

Cited by 8 - [Related Articles](#) - [Web Search](#)

Interrupt protocol system and method using priority-arranged queues of **interrupt status** block ... - all 3 versions »

JT Brady, DW Finney - US Patent 5,606,703, 1997 - Google Patents

... which enables independent **switching** of messages that arrive ... 5 nailing of an **interrupt: internal** node hardware ... order to construct an **Interrupt Status** Block (ISB ...

Cited by 10 - [Related Articles](#) - [Web Search](#)

... for determining adapter **interrupt status** where **interrupt** is sent to host after operating **status** ... - all 3 versions »

GM Nordstrom, DF Moertl, TR Sand - US Patent 6,078,970, 2000 - Google Patents

... [54] SYSTEM FOR DETERMINING ADAPTER **INTERRUPT STATUS** WHERE

INTERRUPT IS SENT TO

HOST AFTER OPERATING **STATUS** STORED IN REGISTER IS SHADOWED TO HOST MEMORY ...

Cited by 8 - [Related Articles](#) - [Web Search](#)

... a stack structure using a single register and a counter to provide transmit **status** in a programmed ... - all 3 versions »

R Hausman, PW Sherer, JP Rivers, C Zikmund, GW ... - US Patent 5,485,584, 1996 - Google Patents

... an **external** coaxial transceiver 260 rather than **internal** twisted pair ... this stack turns off the TX Complete **interrupt** bit in adapter 65 **status** register 350 ...

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[H Fung](#)
[H Oda](#)
[J Prokopik](#)
[D Alexander](#)
[K Johnson](#)

[Integrated circuit having CPU core operable for **switching** between two independent asynchronous clock ... - all 3 versions »](#)

O Oz, G Intrater, Y Afek - US Patent 5,872,960, 1999 - Google Patents

... CIRCUIT HAVING CPU CORE OPERABLE FOR **SWITCHING** BETWEEN TWO ... unit is connected to the

shared **internal** bus and connectable via a shared **external** bus to a ...

[Cited by 7](#) - [Related Articles](#) - [Web Search](#)

[The NMI Absorbed-Dose-to-Water Calorimeter \(A **Status** Report\) - all 2 versions »](#)

M Pieksma, E Van Dijk, AHL Aalbers - Proceedings of the International Workshop on Recent Advances ..., 2000 - npl.co.uk

... 11] Williams AJ and Rosser KE 1998 A **status** report on ... This will establish a new **NMI** calibration facility for ... Jan Seuntjens: You can **switch** it into the loop then ...

[Cited by 3](#) - [Related Articles](#) - [Web Search](#)

[... integrated circuit having DSP module and CPU core operable for **switching** between two independent ... - all 3 versions »](#)

G Intrater, O Oz, Y Afek - US Patent 5,603,017, 1997 - Google Patents

... HAVING DSP MODULE AND CPU CORE OPERABLE FOR **SWITCHING** BETWEEN TWO ... unit is connected

to the shared **internal** bus and connectable via a shared **external** bus to ...

[Cited by 3](#) - [Related Articles](#) - [Web Search](#)

[... dedicated paths for controlling the input and output of data between host processor and **external** ... - all 3 versions »](#)

DJ Lentz, KC Yap - US Patent 5,499,384, 1996 - Google Patents

... provides for the incorporation of an **internal** interrupt controller ... connected to MCU 220 via an **external** bus 262. ... **Switch** network 245 is a means of communicating ...

[Cited by 40](#) - [Related Articles](#) - [Web Search](#)

[Computer activity monitor providing idle thread and other event sensitive clock and power control - all 3 versions »](#)

HTS Fung - US Patent 5,892,959, 1999 - Google Patents

... **NMI** ... is above the idle threshold, T H , the power management software will check the current system **status** and if in the active mode, will **switch** to the ...

[Cited by 22](#) - [Related Articles](#) - [Web Search](#)

[Chip with debug capability - all 3 versions »](#)

J Bengtsson, K Ranerup, P Zander - US Patent 6,502,209, 2002 - Google Patents

... a memory interface units 310A-C and the debug **switch** 136A-C ... 10-15 are used for the CPU interrupt **status** gen-erated ... and **NMI**; 12 No IRQ, no **NMI**; 13 **NMI**, but no ...

[Cited by 2](#) - [Related Articles](#) - [Web Search](#)

[Activity monitor for computer system power management - all 3 versions »](#)

HTS Fung - US Patent 5,799,198, 1998 - Google Patents

... **NMI** ... active mode, will **switch** to the conservation mode, ... 4. The activity monitor 16,



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1 Managing availability: Supporting lightweight negotiations to handle interruptions



Mikael Wiberg, Steve Whittaker

December 2005 **ACM Transactions on Computer-Human Interaction (TOCHI)**, Volume 12
Issue 4

Publisher: ACM Press

Full text available: pdf(2.40 MB)

Additional Information: full citation, abstract, references, index terms

Interruptions are a central aspect of working life. The prevalence of remote co-workers and the use of mobile technology mean that interruptions are more prevalent, and workers have to learn to manage availability. To understand general issues in availability management, we carried out a naturalistic study of how interruptions are handled in face-to-face situations. We found that availability management requires negotiation, that it is also highly dependent on awareness about the availability of ...

Keywords: Availability management, availability negotiation, awareness, interaction asymmetry, interaction management, interruptions, lightweight negotiations, mobile phones

2 The multics system: an examination of its structure

Elliott I. Organick

January 1972 Book

Publisher: MIT Press

Additional Information: full citation, abstract, references, cited by, index terms

This volume provides an overview of the Multics system developed at M.I.T.--a time-shared, general purpose utility like system with third-generation software. The advantage that this new system has over its predecessors lies in its expanded capacity to manipulate and file information on several levels and to police and control access to data in its various files. On the invitation of M.I.T.'s Project MAC, Elliott Organick developed over a period of years an explanation of the workings, concep ...

³ Selected writings on computing: a personal perspective

Edsger W. Dijkstra

January 1982 Book

Publisher: Springer-Verlag New York, Inc.

Additional Information: full citation, abstract, references, cited by, index terms

Since the summer of 1973, when I became a Burroughs Research Fellow, my life has



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switching internal external interrupt NMI

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Relevance scale ☐ ☐ ☐ ☐ ☐**1** [Take a number, stand in line \(interruptions & attention 1\): No task left behind?:](#)[examining the nature of fragmented work](#)

Gloria Mark, Victor M. Gonzalez, Justin Harris

April 2005 **Proceedings of the SIGCHI conference on Human factors in computing systems CHI '05**

Publisher: ACM Press

Full text available: pdf(540.56 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present data from detailed observation of 24 information workers that shows that they experience work fragmentation as common practice. We consider that work fragmentation has two components: length of time spent in an activity, and frequency of interruptions. We examined work fragmentation along three dimensions: effect of collocation, type of interruption, and resumption of work. We found work to be highly fragmented: people average little time in working spheres before switching and 57% of ...

Keywords: attention management, empirical study, information overload, interruptions, multi-tasking

2 [Kernel korner: dynamic interrupt request allocation for device drivers](#)

B. Thangaraju

April 2005 **Linux Journal**, Volume 2005 Issue 132

Publisher: Specialized Systems Consultants, Inc.

Full text available: html(19.11 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

2

3 [Pioneer: verifying code integrity and enforcing untampered code execution on legacy systems](#)

Arvind Seshadri, Mark Luk, Elaine Shi, Adrian Perrig, Leendert van Doorn, Pradeep Khosla

October 2005 **ACM SIGOPS Operating Systems Review , Proceedings of the twentieth****ACM symposium on Operating systems principles SOSP '05**, Volume 39 Issue 5

Publisher: ACM Press

Full text available: pdf(264.30 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We propose a primitive, called Pioneer, as a first step towards verifiable code execution